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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,413	01/26/2005	Hiroji Aga	121797	5555

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ALEXANDRIA, VA 22320

EXAMINER

JEFFERSON, QUOVAUNDA

ART UNIT PAPER NUMBER

2823

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.		Applicant(s)	
	10/522,413		AGA ET AL.	
	Examiner		Art Unit	
	Quovaunda Jefferson		2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, Examiner is unsure what Applicant is referring to in the limitation of "in the separatory ion implanted layer formation step, a depth of formation of the separatory ion implanted layer measured from the ion implantation surface is adjusted through a magnitude of the ion implantation energy in order to adjust a thickness of the bonded silicon single crystal film depending on a thickness of the SOI layer to be obtained, and a dose of the ion implantation is set smaller as the depth of formation of the separatory on implanted layer measured from the ion implantation surface becomes smaller".

In Remarks by Applicant, dated December 21, 2006, Applicant states that they "...found that a smaller amount of dosage of an ion implantation causes separation with a smaller ion implantation depth, The smaller amount of dosage allows a smaller plane

roughness of the separation surface, namely 4.5 nm or less. Therefore, in a case of forming a thin SOI layer, uniformity of layer thickness of the SOI is improved" (page 5 of Remarks). However, Examiner is unsure as to exactly what Applicant is trying to claim as the claim as currently stated does not clearly or effectively show this limitation.

The term "smaller" in claims 1, 3, and 4 is a relative term, which renders the claim indefinite. The term "smaller" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The use of the term "smaller" does not have a clear defining mean. Examiner is unsure as to what specific measurement, range of measurement, or definition of the term that Applicant is referring to in the use of this word.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are the steps necessary to "adjust through a magnitude of an ion implantation energy in order to adjust a thickness of the bonded silicon wafer" and steps of setting "dose of the ion implantation smaller as the depth of formation of the separatory ion implanted layer becomes smaller.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al, US Patent 6,191,007.

Regarding claim 1, Yokokawa teaches a method of fabricating an SOI wafer comprising of an insulating film formation step of forming an insulating film **30** on a first main surface of at least one of a first substrate and a second substrate **21** composed of silicon single crystal, a separatory ion implanted layer formation step of forming a separatory ion implanted layer **40** by implanting ions from an ion implantation surface on the first main surface side of the second substrate, a bonding step of bonding the second substrate having the separatory ion implanted layer formed therein and the first substrate while opposing the first main surfaces with each other, and placing the insulating film in between, a separation step of separating a bonded silicon single crystal film, later becoming an SOI layer, from the second substrate at a position of the separatory ion implanted layer, the separation step forming a separation surface of the

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bonded silicon single crystal film with a roughness (Rms) of 4.5 nm or less [0067] and a planarization step of planarizing having the separation surface side of the bonded silicon single crystal film so as to produce the SOI layer [0009], wherein, in the separatory ion implanted layer formation step, a depth of formation of the separatory ion implanted layer measured from the ion implantation surface is adjusted through a magnitude of an ion implantation energy in order to adjust a thickness of the bonded silicon single crystal film depending on a thickness of the SOI layer to be obtained ([0035] and figure 1).

Yokokawa fails to teach a dose of the ion implantation is set smaller as the depth of formation of the separatory ion implanted layer measured from the ion implantation surface becomes smaller.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions, such as dose of the ion implantation, because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*,

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220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 2, Yokokawa teaches the planarization step further comprises a polishing step of polishing the separation surface side of the bonded silicon single crystal film [0009].

Regarding claim 3, Yokokawa fails to teach in the polishing step, polishing stock removal of the separation surface side of the bonded silicon single crystal film is set smaller as surface roughness of the separation surface of the bonded silicon single crystal film becomes smaller. However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions, such as desired surface smoothness, because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ

143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 4, Matsui fails to teach the dose of the ion implantation is set smaller, and the polishing stock removal, in the polishing step, of the separation surface side of the bonded silicon single crystal film is set smaller, as the thickness of the SOI layer to be obtained becomes smaller. However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claims 5-8, Yokokawa teaches the insulating film is a silicon oxide film [0036].

Response to Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 7AM to 3:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ



FERNANDO L. TOLEDO
PRIMARY PATENT EXAMINER